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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,127	03/15/2004	Daniel A. Chandler	MP1744-US1	3409

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Tyco Electronics Corporation
309 Constitution Drive
Mail Stop R34/2A
Menlo Park, CA 94025

EXAMINER	
BAISA, JOSELITO SASIS	
ART UNIT	PAPER NUMBER
2832	
MAIL DATE	DELIVERY MODE
01/23/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/802,127	CHANDLER ET AL.	
	Examiner	Art Unit	
	JOSELITO BAISA	2832	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,11-15 and 17-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,11-15 and 17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 5, 11, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wartenberg et al. in view of Nagahori [4769901].

Regarding claims 1, 11 and 17, Wartenberg discloses a laminar PTC resistive element 3 having first and second major surfaces and a thickness therebetween;

a first electrode layer 7 formed at the first major surface and being substantially coextensive therewith, and comprising a first metal material of a type adapted to be soldered to a printed circuit substrate for effecting surface mounting of the device;

a second electrode layer 5 formed at the second major surface and being substantially coextensive therewith; and

weld plate [Col. 5, Lines 48-52] means of metal material formed separately of and extending from the second electrode layer and having a volume, thickness and thermal mass capable of withstanding electromechanical interconnect [Col. , Lines 46-48] means without significant resultant damage to the device [Col. 6, Lines 13-19, Figure].

Wartenberg discloses the instant claimed invention discussed above except for the method of interconnecting straps through resistance micro spot welding.

Nagahori discloses spot welding used in attaching lead plate 4a to electrode (weld plate) 3a [Col. 4, Lines 11-33, Figure 1].

It would have been obvious to one having ordinary skill in the art at the time of the invention to use spot welding to connect leads to electrodes as taught by Nagahori to the PTC of Wartenberg.

The motivation would have been to ensure sturdy connection between lead plate and electrode [Col. 4, Lines 11-38, Figures 1-2].

Regarding claim 2, Wartenberg discloses the second electrode layer 5 is formed as a foil layer, and wherein the weld plate means is formed separately of the second electrode layer 5 and is attached thereto by an attachment layer of electrically conductive material [Col. 5, Lines 52-53].

Regarding claim 5, Wartenberg discloses the attachment layer comprises solder [Col. 5, Lines 52-53].

Regarding claim 18, Wartenberg discloses a first tab comprising strap interconnect means capable of being micro spot welded to the weld plate, and a second tab being connected to circuitry of the printed circuit substrate [Col. 5, Lines 28-48].

Claims 3, 4, 12-15 and 18- 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wartenberg et al. in view of Nagahori and further in view of Banich et al. [6104587].

Regarding claims 3, 4, 15 and 20, Wartenberg disclose the instant claimed invention discussed above except for the weld plate comprises nickel.

Banich discloses a weld plate 75 comprises nickel [Col. 5, Lines 8-10].

It would have been obvious to one having ordinary skill in the art at the time of the invention to use a weld plate as taught by Banich to the circuit protection device of Wartenberg.

The motivation would have been to establish electrical stability of the device by using nickel for good adhesion [Col. 5, Lines 1-3].

Regarding claims 12 and 19, Banich discloses the weld plate means has a minimum thickness in a range of 0.100 mm and 0.300 mm [Col. 5, Lines 6-8].

Regarding claim 13, Banich discloses the weld plate has a thickness of approximately 0.250 mm and wherein the strap interconnect means has a thickness not substantially greater than 0.150 mm [Col. 5, Lines 1-8].

Regarding claim 14, Banich discloses the weld plate has a thickness of approximately 0.250 mm and the strap interconnect means has a thickness not substantially greater than approximately 0.250 mm and defines an energy directing opening across which resistance micro spot welds are placed [Col. 5, Lines 1-8].

Allowable Subject Matter

Claims 6-10 and 16 are allowed.

Reason for allowable subject matter:

Claims 6, 16 recite, inter alia, *weld plate means includes a raised central mesa region, and further comprising an insulative box surrounding outer edges of a device and defining an opening exposing the central mesa region.*

The references of record do not teach or suggest the aforementioned

limitation, would it be obvious to modify those references to include such limitation.

Response to Argument

Applicant's arguments with respect to claims 1-5, 11-15 and 17-19 have been considered but are not persuasive.

Applicant argues that the reference Wartenberg does not teach a surface mount circuit protection device should or could have a first electrode layer that is solderable to a printed circuit board and a second electrode layer attached to a weld plate that is capable of withstanding resistance micro spot welding of a strap interconnect means without significant resultant damage to the device. Applicant further stated that Wartenberg merely teaches that metal leads or thermal control elements can be used.

In column 1, lines 47-57, Wartenberg discloses the common application of his device on printed circuit boards as a circuit protection device. In column 5, lines 29-41, Wartenberg discloses a general description of his device. Wartenberg discloses that his invention can be a circuit protection device in which element composed of conductive polymer is in physical and electrical contact with at least one electrode (first or second electrode) suitable for connecting the element to a source of electrical power. The electrode can be a metal foil. The device itself can be of any shape like planar comprising conductive polymer sandwiched between metal foil electrodes. The examiner disagrees.

Wartenberg also discloses additional metal leads in the form of wire or straps can be attached to the foil electrodes to allow connection to a circuit, lines 45-47 of column 5.

Wartenberg further discloses elements to control the thermal output of the device and this can be in a form of metal plates (formed separately) attached to the electrodes. This element conforms to the weld plate of the Applicants claimed invention. This element to control the thermal output of Wartenberg's device has a thermal mass capable of withstanding resistance micro spot welding of a strap.

In conclusion, Wartenberg has a planar circuit protection device with one of its electrode attached to the PCB. The other electrode of the device has a metal plate that controls thermal output (weld plate) where a strap can be attached.

With regards to claims 3, 4, 15 and 20, the Applicant argues that the element 75 of Banich is not comparable to a weld plate as the Applicant has claimed. The examiner disagrees.

Element 75 of Banich is a layer before any other two layers towards the resistive element 3 (conductive polymer). Element 75 can be made of nickel or nickel-alloys, column 5, lines 8-16, and is directly attached to the lead 11. This can be considered weld plate for the reason that it is the layer attached to the lead 11 and not layers 71 and 73. Elements 71, 73 and 75 are layers and therefore are formed separately thus their thickness are considered as what claims 13 and 14 has recited.

With regards to claims 10 and 18, Wartenberg discloses a printed circuit board assembly forms an electrical source (battery) protection circuit module and is mounted to and electrically connected to a strap interconnects, the strap interconnects being micro spot welded to the weld plate means [Col. 5, Lines 28-50].

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joselito Baisa whose telephone number is (571) 272-7132. The examiner can normally be reached on M-F 5:30 am to 2:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Elvin Enad can be reached on (571) 272-1990. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Elvin G Enad/
Supervisory Patent Examiner, Art Unit 2832

Joselito Baisa
Examiner
Art Unit 2832

/J. B./
Examiner, Art Unit 2832